Claims

1. Signal-processing device (1) with an analogue-to-digital converter (3) for the generation of a digital input signal (S_{DE}) from an analogue input signal (S_{AE}), with an intermediate memory (11) for intermediate storage of the digital input signal and a digital signal-processing unit (10) for the digital processing of the digital input signal (S_{DE}) and for the generation of a digital output signal (S_{DA}),

characterised in that

the signal-processing unit (10) can be switched by means of a switching unit (5, 9, 12, 13) in such a manner that the signal-processing unit (10) is series-connected optionally either to the intermediate memory (11) or, by-passing the intermediate memory (11), to the analogue-to-digital converter (3).

2. Signal-processing device according to claim 1,

characterised in that

a resampler (8), which converts the sampling rate f_{ADC} of the analogue-to-digital converter (3) to a lower sampling rate f_{Res} of the signal-processing unit (10), is connected upstream of the signal-processing unit (10).

3. Signal-processing unit according to claim 2,

characterised in that

the resampler (8) has an input low-pass filter (22), of which the unilateral pass bandwidth is 0.2 – 0.3 of the sampling rate f_{Res} of the signal-processing unit (10).

4. Signal-processing device according to any one of claims 1 to 3,

characterised in that,

an up-sampler (20), which inserts a predetermined number of zero values in each case between adjacent sampling values, is arranged between the intermediate memory (11) and the signal-processing unit (10).

5. Signal-processing device according to claim 4,
characterised in that
a switching device (21), with which the up-sampler (20) can be bridged, is provided.

6. Signal-processing device according to any one of claims 1 to 5,
characterised in that
the digital input signal (S_{DE}) is transferred between the analogue-to-digital converter (3) and the intermediate memory (11) on a data bus (15) with an enlarged word width and reduced transfer rate.

7. Signal-processing device according to claim 6,
characterised in that
a packer (6), which increases the word width of the data words of the digital input signal (S_{DE}), is arranged between the analogue-to-digital converter (3) and the intermediate memory (11).

8. Signal-processing device according to claim 7,
characterised in that
an unpacker (16), which reduces the word width and restores the original word width of the data words of the digital input signal (S_{DE}), is arranged at the output of the intermediate memory (11).

9. Signal-processing device according to any one of claims 1 to 8,
characterised in that
the digital output signal (S_{DA}) of the signal-processing device (1) is transferred via an output memory (17) to a host computer (23), with which the signal-processing device (1) co-operates.

S102 a check must be carried out to determine whether an over-range has occurred instead, i.e., a change from polyphase p_{10} in "range 2", with an additional delay of 10 ns in this example caused by the interpolation, to polyphase p_0 in "range 1" from **FIG. 8** with an additional delay of 0.5 ns caused by the interpolation. If this is not the case, then the flow diagram again branches to stage **S100**.

[0043] However, if an over-range is indeed present, only the write pointer, but not the read pointer of the memory element **2** will be adjusted in stage **S103**. As a result of this measure, the delay caused by the memory element **2** is prolonged.

[0044] At the same time, the slide registers of a half-band filter **4** and the delaying elements 6_1, 6_2 and 6_3 of the polyphase filter **5** must be deactivated, so that these do not continue to shift by one clock pulse. After a second interpolation has been carried out in the same range **20** in **FIG. 1B** with the new polyphase, the flow diagram again branches to stage **S100**.

[0045] By contrast with the above, if it is determined in stage **S101** that an under-range is present, then, initially in stage **S104**, which corresponds to **FIG. 4**, a sampled value $S_{in}(k)$ is loaded into the register **30** instead of into the memory element **2**. In this context, the write pointer of the memory element **2** is naturally not adjusted. However, since a sampled value is read out from the memory element **2** at the same time, the read pointer must be adjusted. As a result of this measure, the delay caused by the memory element **2** is reduced. Stage **S104** is represented in **FIG. 4**.

[0046] In stage **S105**, which corresponds to **FIG. 5**, in the next system-clock pulse, both the write pointer and the read pointer are adjusted, but the next sampled value to be written into the memory element **2** is provided with a marking.

[0047] In stage **S106**, normal operation is continued until it is determined in stage **S107** that the marking has arrived at the output of memory element **2**. This means that the additional value stored in the register **30** together with the sampled value x(k) present at the output of the memory element **2** can now be supplied to the delaying element 6_2 of the polyphase filter **5** via the half-band filter **4** and the multiplexer 7_5, as illustrated in **FIG. 6**. The polyphase is changed from 0 ns to 10 ns.

[0048] It must still be pointed out that the runtime of the marked sampled value through the memory element **2** is irrelevant, because the system-clock pulse is substantially greater than the time change in the delay time. In other words, for a given polyphase, a large number of sampled values are interpolated, before changing to the next polyphase. Within this time, the marked sampled value will have arrived at the output of the memory element **2** with a high degree of certainty. In **FIGS. 1B and 1C**, the changes in the delay time are illustrated in an exaggerated manner merely for improved illustration.

[0049] The invention is not restricted to the exemplary embodiment presented. For example, as already mentioned, instead of marking, another procedural control could monitor when the sampled value, which follows the sampled value stored in the register **30**, has arrived at the output of the memory element **2**.

1. Signal delaying device **(1)** for the dynamic delaying of a digitally sampled input signal with a memory element **(2)** and a series connected interpolation element **(3)**, wherein, a register **(30)**, which can be connected to the output side of the interpolation element **(3)** for the intermediate storage of at least one sampled value ($S_{in}(k)$) of the input signal, is arranged in parallel to the memory element **(2)**.

2. Signal delaying device according to claim 1, characterized in that a marking device **(31)** is provided, which, after a sampled value ($S_{in}(k)$) of the input signal has been placed in intermediate storage in the register **(30)**, adds a marking to the next sampled value ($S_{in}(k+1)$) of the input signal stored in the memory element **(2)**.

3. Signal delaying device according to claim 2, characterized in that the interpolation element **(3)** checks whether the marking has arrived at the output of the memory element **(2)**, and following this, reads out a sampled value (x(k)) from the memory element **(2)** and also a sampled value from the register **(30)**.

4. Signal delaying device according to any one of claims **1-3**, characterized in that the interpolation element **(3)** comprises a polyphase filter **(5)**.

5. Signal delaying device according to claim 4, characterized in that the interpolation element **(3)** comprises a half-band filter **(4)**, which is arranged between the memory element **(2)** and the register on one side, and the polyphase filter on the other side.

6. Method for the dynamic delaying of a digitally sampled input signal with the following procedural stages:

storage of the sampled values of the input signal in a memory element **(2)**,

reading out of the sampled values ($S_{in}(k)$) from the memory element **(2)**,

interpolation of the sampled values (x(k)) read out from the memory element **(2)**, wherein

whenever the range **(19)** defined by two successive sampled values (x(k−4), x(k−3)) is neither undercut nor exceeded in the interpolation, one sampled value ($S_{in}(k)$) is placed into the memory element **(2)** and one sampled value (x(k)) is read out from the memory element **(2)**,

whenever the range **(20)** defined by two successive sampled values (x(k−4), x(k−3)) is exceeded in the interpolation, no new sampled value (x(k)) is read out from the memory element **(2)**,

before the range **(21)** defined by two successive sampled values (x(k−4), x(k−3)) is undercut in the interpolation, a sampled value ($S_{in}(k)$) of the input signal is placed in intermediate storage in a register **(30)** arranged in parallel to the memory element **(2)**, the next sampled value ($S_{in}(k+1)$) of the input signal stored in the memory element **(2)** is marked, and a sampled value from the memory element **(2)** and also the sampled value placed in intermediate storage in the register **(30)** are read out, whenever the marked sampled value arrives at the output of the memory element **(2)**.

7. Method according to claim 6, characterized in that the range **(20)** defined by two successive sampled values (x(k−4), x(k−3)) is exceeded, if at least two interpolation values ($S_{out}(k-3)$, $S_{out}(k-2)$) produced by the interpolation fall within this range **(20)**.

8. Method according to claim 6 or 7, characterized in that the range (21) defined by two successive sampled values (x(k−4), x(k−3)) is undercut in the interpolation, if no interpolation value produced by the interpolation falls within this range.

9. Method according to any one of claims 6-7, characterized in that storage in the memory element (2) takes place by means of a write pointer, and reading out from the memory element (2) takes place by means of a read pointer, wherein the write pointer and the read pointer in each case point towards a given memory cell of the memory element,

wherein the write pointer and also the read pointer are adjusted if the range (19) defined by two successive sampled values (x(k−4), x(k−3)) is neither undercut nor exceeded in the interpolation.

10. Method according to claim 9, characterized in that only the write pointer but not the read pointer is adjusted, if the range (20) defined by two successive sampled values (x(k−4), x(k−3)) is exceeded in the interpolation.

11. Method according to claim 9 characterized in that only the read pointer but not the write pointer is adjusted, if a sampled value is stored in the register (30).

12. Method according to claim 9, characterized in that both the write pointer and also the read pointer are adjusted, if a sampled value is read out from the register (30).

* * * * *

[0121] which permits these statements:

$$P_{MESS,sin}=P_{sin}\cdot(G_{DUT}\cdot G_M)=P_{sin}\cdot G_{ges} \quad (34)$$

$$P_{MESS,Noise}=k\cdot T_{ges}\cdot B_M\cdot(G_{DUT}\cdot G_M)=k\cdot T_{ges}\cdot B_M\cdot G_{ges} \quad (35)$$

[0122] whence the following is derived:

$$T_{ges}=\frac{P_{sin}}{k\cdot B_M}\cdot\frac{P_{MESS,Noise}}{P_{MESS,sin}}\gg T_{DUT} \quad (36)$$

$$G_{ges}=\frac{P_{MESS,sin}}{P_{sin}}\approx G_{DUT} \quad (37)$$

[0123] The bandwidth of the measuring apparatus B_M must be known exactly. With modern measuring apparatuses this is no problem, since the bandwidths are produced either entirely digitally or are calibrated.

[0124] In the following, a more precise determination of the noise. temperature T_{DUT} of the object to be measured **2** is given with consideration paid to a calibration made prior to the measurement.

[0125] Given the following described items in **FIG. 8** and **FIG. 9**:

P_{sin}	level of the sine reference source 1
$P_{CAL,sin}$	measured sine level at the calibration
$P_{MESS,sin}$	measured sine level at the measurement
$P_{CAL,noise}$	measured noise power at the calibration
$P_{MESS,noise}$	measured noise power at the measurement
G_{DUT}	amplification of the object to be measured 2
B_{DUT}	band width of the object to be measured 2
G_M	amplification of the measurement apparatus (level meter) 3
B_M	bandwidth of the measurement apparatus (level meter) 3

[0126] The following equations can be established:

$$P_{CAL,sin}=P_{sin}\cdot G_M \quad (38)$$

$$P_{CAL,noise}=k\cdot T_M\cdot B_M\cdot G_M \quad (39)$$

$$P_{MESS,sin}=P_{sin}\cdot(G_{DUT}\cdot G_M)=P_{sin}\cdot G_{ges} \quad (40)$$

$$P_{MESS,noise}=k\cdot T_{ges}\cdot B_M\cdot(G_{DUT}\cdot G_M)=k\cdot T_{ges}\cdot B_M\cdot G_{ges} \quad (41)$$

[0127] The noise power of the entire system permits the following to be presented:

$$P_{noise,ges}=\underbrace{k\cdot B_M\cdot T_{ges}\cdot(G_{DUT}\cdot G_M)}_{System}=\underbrace{k\cdot B_M\cdot T_{DUT}\cdot(G_{DUT}\cdot G_M)}_{Object\ to\ be\ measured}+\underbrace{k\cdot B_M\cdot T_M\cdot G_M}_{Measuring\ instrument} \quad (42)$$

$$T_{ges}=T_{DUT}+\frac{T_M}{G_{DUT}} \quad (43)$$

[0128] With the formulae (38) to (43) there is made available the noise temperature T_{DUT} and the amplification G_{DUT} of the object to be measured **2**, with the following equations:

$$T_{DUT}=\frac{P_{sin}}{k\cdot B_M}\cdot\frac{(P_{MESS,noise}-P_{CAL,noise})}{P_{MESS,sin}} \quad (44)$$

-continued

$$G_{DUT}=\frac{P_{MESS,sin}}{P_{CAL,sin}} \quad (45)$$

[0129] The invented procedure and the apparatus enables a very accurate measurement for both the noise temperature as will and the amplification of the object to be measured. Further it is of advantage, that the noise value magnitudes can be measured even at a high excitation of the object to be measured. For instance, an amplifier in the full modulated state can be measured, which is not possible with the procedure in accord with the state of the technology.

Claimed is:

1. A procedure for the determination of the magnitude of a noise (T_{DUT}) of an electronic object to be measured (**2**) by the input of a sine signal (S_{in}) and the measurement of an associated power level by means of a level meter (**3**), therein characterized, in that by means of the level meter (**3**), a sine power level (P_{sin}) and a noise power level (P_{noise}) are separately determined.

2. A procedure in accord with claim 1, therein characterized, in that the level meter (**3**) takes the sample of the output signals (S_{out}) and in that, from the sine power level, (P_{sin}) by taking the arithmetical average in device (**33**), the samples and subsequent squaring (**34**) of the amount of the arithmetical average (AVG), the sample value may be determined.

3. A procedure in accord with claim 2, therein characterized, that the noise power level can be obtained by taking the arithmetical average (**35**) of the amount squared of the samples and subsequent subtraction of the sine power level (P_{sin}).

4. A procedure in accord with claim 2 or **3**, therein characterized, in that prior to taking the average value (**33**, **35**), an estimation (**28**) and a revision (**29**) of a deviation of the frequency of an input sine signal (S_{in}) from the frequency of an available local oscillator (**22**) in the level meter (**3**) is carried out.

5. A procedure in accord with one of the claims 1 to 4, therein characterized, in that the magnitude of the noise is the noise temperature T_{DUT} of the object to be measured **2**, and the noise temperature T_{DUT} can be determined by the formulae:

$$T_{DUT}=\frac{P_{sin}}{k\cdot B_M}\cdot\frac{P_{MESS,noise}}{P_{MESS,sin}}$$

whereby

P_{sin}	the power level of the sine signal at the input of the object to be measured (2)
$P_{MESS,sin}$	the sine power level measured with the level meter (3)
$P_{MESS,noise}$	the noise power level measured with the level meter (3)
k	the Boltzmann Constant, and
B_M	the bandwidth of the level meter (3)

are defined as they appear in the above equation.

6. A procedure in accord with one of the claims 1 to 4, therein characterized, in that, a calibration precedes the measurement, in which the sine signal (S_{in}) has the same level as is the case with the measurement, however, circuitously by-passing the object to be measured (2) the said sine signal (S_{in}) is input directly into the level meter (3) and in that the magnitude of the noise is the noise temperature T_{DUT} and the noise temperature T_{DUT} of the object to be measured (2) is determined by the formula:

$$T_{DUT} = \frac{P_{sin}}{k \cdot B_M} \cdot \frac{(P_{MESS,noise} - P_{CAL,noise})}{P_{MESS,sin}}$$

wherein

P_{sin}	the power level of the sine signal at the input to the object to be measured (2),
$P_{MESS,sin}$	the power level of the sine measured with intermediate circuitous inclusion of the object to be measured (2) and measured with the level meter (3)
$P_{MESS,Noise}$	the power level of the noise measured with intermediate circuitous inclusion of the object to be measured (2) measured with the level meter (3)
$P_{CAL,noise}$	the power level of the noise measured without intermediate circuitous inclusion of the object to be measured (2) measured with the level meter (3)
k	the Boltzmann Constant
B_M	the bandwidth of the level meter (3).

7. An apparatus for the determination of a magnitude of a noise (T_{DUT}) of an electronic object to be measured (2) with a sine-signal source (1), which produces a sine signal (S_{in}) which is to be input into the object to be measured (2), and a level meter (3) for the measurement of a power level at the output of the object to be measured (2), therein characterized, in that the level meter (3) is equipped with a sine power level detector device (31) for the separate and discrete capture of a sine power level $\hat{P}_{sin}$ and a noise power level detector device (32) for the capture of a noise power level ($\hat{P}_{noise}$).

8. An apparatus in accord with claim 7, therein characterized, in that the level meter (3) captures the samples of the output signal (S_{out}) at the object to be measured (2) and in that the sine power level detector device (31) determines the sine-power level $\hat{P}$sin by taking the arithmetical average (33) of the sample and subsequent squaring (34) of the amount of the arithmetic average value (AVG) of the sample.

9. An apparatus in accord with claim 8, therein characterized, in that the noise power level detector device (32) determines the noise power level ($\hat{P}_{noise}$) by taking the arithmetical average (35) of the square of the amount of the sample and subsequent subtraction (36) of the sine power level $\hat{P}_{sin}$.

10. An apparatus in accord with claim 8 or 9, therein characterized in that the level meter (3) has a frequency estimation device (28) which, prior to taking the average (33, 35) undertakes an estimation of a frequency deviation between the frequency of the sin signal (S_{in}) input into the object to be measured (2) and the frequency of a local oscillator (22) present in the level meter (3), and a frequency correction device (29), which rectifies the said frequency deviation.

11. An apparatus in accord with one of the claims 7 to 10, therein characterized, in that the magnitude of the noise is the noise temperature T_{DUT}, and an evaluator (40) determines the noise temperature T_{DUT} of the object to be measured by means of the formula:

$$T_{DUT} = \frac{P_{sin}}{k \cdot B_M} \cdot \frac{(P_{MESS,noise})}{P_{MESS,sin}}$$

wherein the following symbols represent:

$P_{(sin)}$	the power level of the sine signal at the input of the object to be measured (2),
$P_{(MESS,sin)}$	the sine power level as measured with the level meter (3),
$P_{MESS,noise}$	the noise power level as measured with the level meter (3),
k	the Boltzmann Constant, and
B_M	the bandwidth of the level meter (3)

12. An apparatus in accord with one of the claims 7 to 11, therein characterized in that a calibration precedes the measurement, in the case of which the sin signal $P_{(sin)}$ is input directly into the level meter (3) at the same level as determined by the measurement, however, without an intermediate routing through the object to be measured (2) and in that the magnitude of the noise is the noise temperature T_{DUT} and an evaluation device (40) determines the noise temperature T_{DUT} of the object to be measured in accord with the formula:

$$T_{DUT} = \frac{P_{sin}}{k \cdot B_M} \cdot \frac{(P_{MESS,noise} - P_{CAL,noise})}{P_{MESS,sin}}$$

wherein the following symbols represent:

P_{sin}	the power level of the sine signal at the input of the object to be measured (2),
$P_{MESS,sin}$	the sine power level with circuitous inclusion of the object to be measured (2) as measured with the level meter (3),

-continued

$P_{MEAS,noise}$	the noise power level with circuitous inclusion of the object to be measured (2), as measured with the level meter (3),
$P_{CAL,noise}$	the noise power level without circuitous inclusion of the object to be measured (2), as measured with the level meter (3),

-continued

k	the Boltzmann Constant, and
B_M	the bandwidth of the level meter (3)

* * * * *

Linear interpolation is performed among these tabulated function values. The straight lines used for the interpolation are shown in **FIG. 7**. It can be seen that the linear increase is always independent of the position of the index. **FIG. 3** makes it apparent that it is more advantageous with regard to tabular error $\epsilon_{TAB}(i)/K$ to store the function values in storage device **20**, not at the indices x_i, x_{i+1}, etc., but at the positions between them, i.e., for example at the position $(x_i+x_{i+1})/2$. This reduces the tabular error $\epsilon_{TAB}(i)/K$ by half.

[0042] When a uniform, constant increase m_{const} is used for linear interpolation over the entire compressed argument range, then it can be demonstrated, for the case in which the mathematical function is the logarithm to the base 2 and the compressed argument range lies between 0.5 and 1, that for the constant increase m_{const} at which the lowest maximum interpolation error occurs:

$$m_{const}=3/(2\cdot\ln 2)=2.164 \tag{13}$$

[0043] However, the rounded constant increase $m_{const}=2$ is easier to implement. The error in the output signal $y_{LOG}(x)$ that arises when $m_{const}=2$ is depicted in **FIG. 5** as a function of first intermediate signal A.

[0044] As mentioned hereinabove, the interpolation error can be reduced still further by dividing the argument range into multiple segments I_1, I_2, I_3, with an increase that is constant within each segment but differs from one segment to the next. For example, the compressed argument range [0.5, 1) can be divided into the segments

$$I_1:\frac{1}{2}\le A<\frac{5}{8} \tag{14}$$

$$I_1:\frac{5}{8}\le A<\frac{3}{4}$$

$$I_1:\frac{3}{4}\le A<1$$

[0045] For these range limits $A_1=5/8$, $A_2=3/4$, depicted in **FIG. 6**, it can be shown that the optimum increase to be used for linear interpolation in the three different segments I_1, I_2 and I_3 can be expressed by:

$$I_1:m_{const,1}=\frac{9}{5\cdot\ln 2}\cdot\approx 2,5969\approx 2,625=2+2^{-1}+2^{-3} \tag{15}$$

$$I_2:m_{const,2}=\frac{22}{15\cdot\ln 2}\cdot\ln 2\approx 2,1160\approx 2,125=2+2^{-3}$$

$$I_3:m_{const,3}=\frac{7}{6\cdot\ln 2}\approx 1,6831\approx 1,625=1+2^{-3}$$

[0046] The rounded values can be represented as a combination of integral powers of 2, and thus the multiplication operations performed during the linear interpolation can be performed by bit shifting without placing very great demands on the hardware.

[0047] Although the index width Δx used in the example of **FIG. 6** was four times that of the example of **FIG. 5**, the error did not increase substantially.

[0048] The implementation for the aforesaid example is shown in **FIG. 4**. The less significant bits, which are not included in the address word ADR, form the data word A-ADR and are routed to an interpolator **30**. A subtractor **21** of the interpolator subtracts from the data word A-ADR the value $\Delta x/2$ that occurs in each case, Δx being the distance between two indices. This allows for the circumstance noted in reference to **FIG. 3**, that the function values B1 are each tabulated between the indices, making this correction necessary.

[0049] The output of subtractor **21** is connected to a first multiplexer **23** both directly and via a bit shifter **22** that increases the significance of the output values of subtractor **21** by one position at a time. The output of subtractor **21** is further connected, via a second bit shifter **24** that decreases the significance of the bits from the output of subtractor **21** by one position at a time, to a second multiplexer **25** to the other output of which the data value "0" is constantly supplied. Via a third bit shifter **26**, which decreases the bits representing the output values of subtractor **21** by three positions, a first input of a first adder **27** is connected to the output of subtractor **21**. The other input of the first adder **27** is connected to the output of the second multiplexer **25**. A first input of a second adder **28** is connected to the output of first adder **27**, while a second input of second adder **28** is connected to the output of first multiplexer **23**. The interpolation values B2 are available at the output of second adder **28**. The function value B1 read from storage device **20** and the interpolation values B2 are supplied to the inputs of a third adder **29**. The second intermediate signal B is then available at the output of third adder **29**.

[0050] Multiplexers **23** and **25** perform the task of switching among the mutually different but intrasegmentally constant increases $m_{const.3}$, $m_{const.2}$ and $m_{const.1}$ in dependence on the exemplary values given hereinabove. For this purpose, multiplexer **23** connects the input labeled "1" to its output if the eighth bit, ADR(8), of the address word ADR is not set. Otherwise, the input of first multiplexer **23** labeled "0" is connected to its output. Second multiplexer **25** connects its input labeled "1" to its output if the eighth bit, ADR(8), of the address word ADR is not set or the seventh bit, ADR(7), of the address word ADR is set. As can be seen from simple logical combination, this implements the exemplary values given in Eqs. (15) for the different increases in the various segments I_1, I_2, I_3 of the compressed argument range. Bit shifters **22**, **24**, **26**, multipliers **23**, **25** and adders **27**, **28** thus form a switchable multiplication system **31**.

[0051] The invention is not limited to the exemplary embodiment described, and also lends itself to any desired mathematical functions. The invention can be implemented both as hardware in the form of an electronic circuit, especially an FPGA (free-programmable gatter array), and as software, for example in a digital signal processor.

[0052] While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A method for generating a digital output signal ($y_{LOG}(k)/K$) as a mathematical function of a digital input signal ($X_{LOG}(k)$) with the aid of a computer, a digital signal processor or an electronic circuit, comprising the following method steps:

amplifying or attenuating the input signal ($x_{LOG}(k)$) to generate a first intermediate signal (A) that falls within a compressed argument range of said mathematical function, and a correction signal ($Shift_{LOG}$) dependent on said amplification or attenuation of said input signal ($x_{LOG}(k)$),

reading from a table function values (B1) tabulated at or between indices (x_i, x_{i+1}, y_i, y_{i+1}) in dependence on said first intermediate signal (A) and generating a second intermediate signal (B) in dependence on the read tabulated function values (B1) and

generating said digital output signal ($y_{LOG}(k)/K$) by correcting said second intermediate signal (B) by means of said correction signal ($Shfit_{LOG}$).

2. The method as recited in claim 1, characterized by

generating interpolation values (B2) in dependence on the deviation of said first intermediate signal (A) from said indices (x_i, x_{i+1}, y_i, y_{i+1}) and generating said second intermediate signal (B) by summing said read tabulated function values (B1) and said interpolation values (B2).

3. The method as recited in claim 2, characterized in that

a linear interpolation is performed using an increase m_{const} that is constant within said compressed argument range.

4. The method as recited in claim 3, characterized in that

the constant increase m_{const} is so selected that the interpolation error that occurs during the interpolation is as small as possible.

5. The method as recited in claim 4, characterized in that

said mathematical function is the logarithm to the base 2, said compressed argument range is between 0.5 and 1, and said constant increase is $m_{const}=2$.

6. The method as recited in claim 2, characterized in that

a linear interpolation is performed using increases $m_{const.1}$, $m_{const.2}$ and $m_{const.3}$ that are constant within segments between range limits (A_1, A_2).

7. The method as recited in claim 6, characterized in that

said constant increases $m_{const.1}$, $m_{const.2}$, $m_{const.3}$ are so selected that the interpolation error that occurs during interpolation is as small as possible.

8. The method as recited in claim 7, characterized in that

said mathematical function is the logarithm to the base 2, said compressed argument range is between 0.5 and 1, and said constant increases are $m_{const.1}=2+2^{-1}+2^{-3}$, $m^{const.2}=2+2^{-3}$ and $m_{const.3}=1+2^{-3}$.

9. The method as recited in any of claims 1 to 8, characterized in that

said digital input signal ($x_{LOG}(k)$) consists of a real component (I) and an imaginary component (Q) that are squared and summed before being acted upon by said mathematical function.

10. The method as recited in claim 9, characterized in that

said amplification or attenuation of said digital input signal ($x_{LOG}(k)$) takes place at least in part before the squaring of said components (I, Q) of said digital input signal ($x_{LOG}(k)$).

11. The method as recited in any of claims 1 to 10, characterized in that

said mathematical function is the logarithm to a specified base and said correction signal ($Shift_{LOG}$) represents the exponent (x) of the same base of an amplification factor (2^x) used for the amplification and said correction is made by subtracting said correction signal ($Shift_{LOG}$) from said second intermediate signal (B).

12. A device (1) for generating a digital output signal ($y_{LOG}(k)/K$) as a mathematical function of a digital input signal ($x_{LOG}(k)$), comprising

a level-changing device (6) which by amplifying or attenuating the input signal ($x_{LOG}(k)$) generates a first intermediate signal (A) that falls within a compressed argument range of said mathematical function, and a correction signal ($Shift_{LOG}$) that depends on the amplification or attenuation of said input signal ($x_{LOG}(k)$),

a storage device (20) in which function values of said mathematical function are stored at or between indices (x_i, x_{i+1}; y_i, y_{i+1}), the tabulated function values (B1) being read from said storage device (20) in dependence on said first intermediate signal (A) and a second intermediate signal (B) being generated in dependence on the read tabulated function values (B1), and

a correcting element (12) that generates said digital output signal ($y_{LOG}(k)/K$) by correcting said second intermediate signal (B) by means of said correction signal ($Shift_{LOG}$).

13. The device as recited in claim 12, characterized by

an interpolator (30) that generates interpolation values (B2) in dependence on the deviation of said first intermediate signal (A) from said indices (x_i, x_{i+1}, y_i, y_{i+1}), and

an adder (29) that sums said tabulated function values (B1) and said interpolation values (B2).

14. The device as recited in claim 13, characterized in that

in said interpolator (30) a linear interpolation is performed using increases $m_{const.1}$; $m_{const.2}$, $m_{const.3}$) that are each constant within segments (I_1, I_2, I_3) of said compressed argument range, and

a switchable multiplication system (31) is provided, which multiplies a multiplier (A-ADR-Δx/2) corresponding to the deviation of said first intermediate signal (A) from reference positions ($(x_i+x_{i+1})/2$, (y_i, y_{i+1})/2)) defined by the indices (x_i, x_{i+1}, y_i, y_{i+1}), depending on the segment (I_1, I_2, I_3) in which said intermediate signal (A) is located, by the constant increase ($m_{const.1}$, $m_{const.2}$, $m_{const.3}$) appertaining to the segment (I_1, I_2, I_3) concerned.

15. The device as recited in claim 14, characterized in that

said switchable multiplication system (31) comprises bit shifters (22, 24, 26) that shift the significance of the bits of said multiplier (A-ADR-Δ/2), multiplexers (23, 25) and adders (27, 28).

16. The device as recited in any of claims 12 to 15, characterized in that

a square generator (2) is provided, which squares a real component (1) and an imaginary component (Q) of said digital input signal ($x_{LOG}(k)$) and sums the squared components.

17. The device as recited, in claim 16, characterized in that

said level-changing device (6) comprises a first level-changing subdevice (6*a*) disposed before the input of said square generator (2) and a second level-changing subdevice (6*b*) disposed after the output of said square generator (2), and said correction signal ($Shift_{LOG}$) is composed of a first correction subsignal ($Shift_{IQ}$) generated by said first level-changing subdevice (6*a*) and a second correction subsignal ($Shift_{CORR}$) generated by said second level-changing subdevice (6*b*).

18. The device as recited in any of claims 12 to 17, characterized in that

said mathematical function represents the logarithm to a specified base and said correction signal ($Shift_{LOG}$) represents the exponent (x) of the same base of an amplification factor (2^x) used in said level-changing device, and

said correcting element is a subtractor (12) that subtracts said correction signal ($Shift_{LOG}$) from said second intermediate signal (B).

19. A computer program comprising program-code means enabling it to perform all the steps recited in any of claims 1 to 11 when the program is executed on a computer or a digital signal processor.

20. A computer program comprising program-code means enabling it to perform all the steps recited in any of claims 1 to 11 when the program is stored on a machine-readable data carrier.

21. A computer program product comprising program-code means stored on a machine-readable carrier and enabling it to perform all the steps recited in any of claims 1 to 11 when the program is executed on a computer or a digital signal processor.

* * * * *

CLAIM SET AS AMENDED

1. (currently amended) A method for estimating one of the frequency (f_{a1}) and the phase (ϕ_{a1}) of a digital input signal (x(i)) having the following process steps:

- determining phase values ($C_{a1}(i)$) of the digital input signal (x(i)),

- summing the phase values ($C_{a1}(i)$) over a predetermined summation length N/B, which is a predetermined fraction 1/B of an observation length of N phase values ($C_{a1}(i)$), to create added-up phase values ($S_{a1}(i)$), where B is a posibe integer,

- reducing a sampling rate of the added-up phase values ($S_{a1}(i)$) by the factor N/B in comparison with a sampling rate (f_{a2}) of the phase values ($C_{a1}(i)$),

- delaying the added-up phase values ($S_{a1}(i)$) with at least B-1 delay elements, each of which delays the added-up phase values ($S_{a1}(i)$) by one sampling period of the reduced sampling rate ($f_{a2} \bullet B/N$),

- adding up the delayed ~~differently delayed~~ added-up phase values ($S_{a1}(i)$) to create a resulting pulse response (h_f) of the frequency so that one of the resulting pulse responses (h_f) of the frequency (f_{a1}) is constant positive in a first interval [[(40)]], is zero in a second interval [[(41)]], and is constant negative in a third interval (42), and such that a [[the]] resulting pulse response

(h_ϕ) of the phase ~~that~~ is constant in at least a middle interval [[(43)]] of the observation length [[(N)]] and is otherwise zero.

2. (currently amended) The method of claim 1, wherein the fraction 1/B is 1/(3•n), where n is a positive [[an]] integer.

3. (currently amended) The method of claim 2, wherein the fraction 1/B is 1/3, wherein a first delay element and second delay element ~~two delay elements (15, 16)~~ are provided, and wherein the added-up phase value ($S_{a1}(i-2)$) at the output of the second delay element ~~(16)~~ is subtracted from the added-up phase value ($S_{a1}(i)$) at the input of the first delay element ~~(15)~~ to determine the estimated frequency (f_{a1}).

4. (currently amended) The method of claim 2, wherein the fraction 1/B is 1/3, wherein a first delay element and second delay element ~~two delay elements (15, 16)~~ are provided, and wherein the added-up phase value ($S_{a1}(i)$) at the input of the first delay element [[(15)]], the added-up phase value ($S_{a1}(i)$) at the output of the first delay element, [[(15)]] and the added-up phase value ($S_{a1}(i-2)$) at the output of the second delay element [[(16)]] are summed to determine the estimated phase (ϕ_{a1}).

5. (currently amended) The method of claim 2 [[3]], wherein the

fraction 1/B is 1/6, wherein a first, second, third, fourth, and fifth ~~five~~ delay elements ~~(26-30)~~ are provided, and wherein the added-up phase value at the input of the first delay element [[(26)]] and the added-up phase value ($S_{a1}(i-1)$) at the output of the first delay element [[(26)]] are added, and from this the added-up phase values ($S_{a1}(i-4)$) at the output of the fourth delay element [[(29)]] and ($S_{a1}(i-5)$) at the output of the fifth delay element [[(30)]] are subtracted to determine the estimated frequency (f_{a1}).

6. (currently amended) The method of claim 2 [[4]], wherein the fraction 1/B is equal to 1/6, wherein a first, second, third, fourth, and fifth ~~five~~ delay elements ~~(26-30)~~ are provided, and the added-up phase values ($S_{a1}(i-1)$) at the output of the first delay element [[(26)]], ($S_{a1}(i-2)$) at the output of the second delay element [[(27)]], ($S_{a1}(i-3)$) at the output of the third delay element [[(28)]] and ($S_{a1}(i-4)$) at the output of the fourth delay element [[(29)]] are summed to determine the estimated phase (ϕ_{a1}).

7. (currently amended) The method of claim 1, wherein each of the first interval ~~intervals~~ [[(40)]], the second interval, [[(41)]] and the third interval [[(42)]] of the resulting pulse response (h_f) of the frequency has a length of N/B, in particular 1/3 N.

8. (currently amended) The method of claim 1, wherein the middle interval [[(43)]] of the resulting pulse response (h_ϕ) of the phase has the length $N \bullet (3n-n)/3 \bullet n$, in particular 2/3 N, where n is a positive integer.

9. (currently amended) The method of claim 1, wherein the middle interval [[(43)]] of the resulting pulse response (h_ϕ) extends over the total observation length N.

10. (currently amended) An apparatus for estimating the frequency (f_{a1}) and/or the phase (ϕ_{a1}) of a digital input signal (x(i)), the apparatus comprising:

- a phase determining device, [[(3)]] which determines phase values ($C_{a1}(i)$) of the digital input signal (x(i)),
- a first filter [[(4)]], which adds up the phase values ($C_{a1}(i)$) over a predetermined summation length N/B, which is a predetermined fraction 1/B of an observation length of N phase values ($C_{a1}(i)$), to form added-up phase values ($S_{a1}(i)$), and the sampling rate of the added-up phase values ($S_{a1}(i)$) is reduced by a factor N/B in comparison with a sampling rate (f_{a2}) of the phase values ($C_{a1}(i)$),
- a second filter [[(8)]] which delays the added-up phase values ($S_{a1}(i)$) in a chain of at least B-1 delay elements ~~(15, 16; 26-30)~~, which respectively delay the added-up phase values ($S_{a1}(i)$) by one sampling period of the reduced sampling rate ($f_{a2} \bullet B/N$), and adds or

subtracts the ~~differently delayed~~ delayed added-up phase values $(S_{a1}(i))[[,]]$ to create a resulting pulse response (h_f) of the frequency so that at least one of: a resulting pulse response (h_f) of the frequency is constant positive in a first interval [[(40)]], is zero in a second interval, or [[(41)]] ~~and~~ is constant negative in a third interval, ~~(42),~~ and wherein ~~they are added to create~~ a resulting pulse response (h_ϕ) of the phase is created so that the resulting pulse response (h_ϕ) of the phase is constant in at least a middle interval [[(43)]] and is otherwise zero.

11. (currently amended) The apparatus of claim 10, wherein the phase determination device [[(3)]] has a counter [[(24)]] whose count is read out at a constant sampling rate (f_{a2}).

12. (currently amended) The apparatus of claim 10, wherein the first filter [[(4)]] has an integrator [[(10)]], a differentiator [[(11)]] and a first sampling-rate converter [[(14)]] arranged between the integrator [[(10)]] and the differentiator [[(11)]] to reduce the sampling rate of the added-up phase values ($S_{a1}(i)$) by the factor N/B in comparison with the sampling rate frequency (f_{a2}) of the phase values ($C_{a1}(i)$).

13. (currently amended) The apparatus of claim 10, wherein the fraction 1/B is 1/3, and the second filter [[(8)]] has a first

delay element and a second delay element ~~two delay elements (15, 16)~~ and a subtractor, [[(18)]] which subtracts the added-up phase values ($S_{a1}(i-2)$) at the output of the second delay element [[(16)]] from the added-up phase values ($S_{a1}(i)$) at the input of the first delay element [[(15)]] to determine the estimated frequency (f_{a1}).

14. (currently amended) The apparatus of claim 10, wherein the fraction 1/B is 1/3, and the second filter [[(8)]] has a first delay element and a second delay element ~~two delay elements (15, 16)~~ and adders ~~(20, 21)~~ which sum the added-up phase values ($S_{a1}(i)$) at the input of the first delay element [[(15)]], the added-up phase values ($S_{a1}(i-1)$) at the output of the first delay element, [[(15)]] and the added-up phase values ($S_{a1}(i-2)$) at the output of the second delay element [[(16)]] to determine the estimated phase (ϕ_{a1}).

15. (currently amended) The apparatus of claim 13, wherein a second sampling-rate converter ~~(37, 23)~~ is arranged to follow at least one of the adders ~~(20, 21)~~ and the subtractor [[(18)]] to reduce the sampling rate by a factor of 3.

16. (currently amended) The apparatus of claim 10, wherein the fraction 1/B is 1/6, and the second filter [[(8)]] has a first, second, third, fourth, and fifth ~~five~~ delay elements ~~(26-30)~~, an

adder [[(31)]] that adds up the added-up phase values ($S_{a1}(i)$) at the input of the first delay element [[(26)]] and the added-up phase values ($S_{a1}(i-1)$) at the output of the first delay element [[(26)]], and subtractors ~~(32, 33)~~ which subtract therefrom the added-up phase values ($S_{a1}(i-4)$) at the output of the fourth delay element [[(29)]] and the added-up phase values ($S_{a1}(i-5)$) at the output of the fifth delay element [[(30)]] to determine the estimated frequency (f_{a1}).

17. (currently amended) The apparatus of claim 10, wherein the fraction 1/B is 1/6, and the second filter [[(8)]] has a first, second, third, fourth, and fifth ~~five~~ delay elements ~~(26-30)~~ and adders ~~(34-36)~~ which add up the added-up phase values ($S_{a1}(i-1)$) at the output of the first delay element [[(26)]], the added-up phase values ($S_{a1}(i-2)$) at the output of the second delay element [[(27)]], the added-up phase values ($S_{a1}(i-3)$) at the output of the third delay element [[(28)]] and the added-up phase values ($S_{a1}(i-4)$) at the output of the fourth delay element [[(29)]] to determine the estimated phase (ϕ_{a1}).

18. (currently amended) The apparatus of claim 16, wherein a second sampling-rate converter ~~(37, 23)~~ is respectively arranged after at least one of the adders ~~(34, 36)~~ and the subtractors ~~(32, 33)~~ for reducing the sampling rate by a factor of 6.